IN THE CLAIMS

1 (Currently Amended). A method comprising:

forming a phase change memory pore including a breakdown layer in said pore and increasing the likelihood that a ~~the~~ breakdown will occur in one region of said breakdown layer in said pore rather than another region of said breakdown layer in said pore.

2 (Currently Amended). The method of claim 1 including forming a phase change memory pore by:

forming an electrode over a substrate;

forming a dielectric layer with an ~~aperature~~ aperture; and

forming a breakdown layer over said electrode in said aperture.

3 (Original). The method of claim 2 including forming a phase change material over said layer and coupling said phase change material between an upper conductive line and a lower conductive line.

4 (Currently Amended). The method of claim 3 including coupling ~~a~~ the lower conductive line to said electrode through a selector device.

5 (Original). The method of claim 1 including ion implanting a portion of said layer to change the likelihood of breakdown in that implanted portion relative to an unimplanted portion of said layer.

6 (Original). The method of claim 5 including implanting at an angle.

7 (Original). The method of claim 6 including forming a pore defined in an insulator and implanting at an angle such that said insulator acts as a mask to said ion implantation.

8 (Previously Presented). The method of claim 1 including forming a relatively centrally located region within said pore that is more likely to breakdown.

9 (Original). The method of claim 1 including forming a relatively peripherally located region in said pore that is more likely to breakdown.

10 (Original). The method of claim 1 including damaging one region of said layer to change the likelihood that a breakdown will occur in that region relative to another region.

11 (Currently Amended). A memory comprising:

a breakdown layer between a pair of electrodes, said breakdown layer being ion implanted to increase the likelihood that a breakdown will occur in one region rather than another region of said layer.

12 (Original). The memory of claim 11 wherein said memory is a phase change memory including a phase change material between said electrodes.

13 (Original). The memory of claim 12 wherein said phase change material is a chalcogenide.

14 (Original). The memory of claim 13 including a substrate and a dielectric layer over said substrate with an aperture formed therein, an electrode being positioned at the bottom of said aperture and said breakdown layer being positioned over said electrode in said aperture.

15 (Original). The memory of claim 14 wherein said phase change material is over said breakdown layer.

16 (Original). The memory of claim 15 including an upper conductive line over said phase change material and a lower conductive line under said electrode.

17 (Original). The memory of claim 11 wherein said breakdown layer is formed of an insulator.

18 (Original). The memory of claim 17 wherein said insulator includes nitride.

19 (Original). The memory of claim 11 wherein a central portion of said layer is ion implanted and a peripheral region of said breakdown layer is not ion implanted.

20 (Currently Amended). A system comprising:

a processor-based device;

a wireless interface coupled to said processor-based device; and

a semiconductor memory coupled to said device, said memory including a pair of electrodes, a breakdown layer between said pair of electrodes, said breakdown layer being ion implanted to increase the likelihood that a breakdown will occur in one region rather than another region of said layer.

21 (Original). The system of claim 20 wherein said memory is a phase change memory including a phase change material between said electrodes.

22 (Original). The system of claim 21 wherein said phase change material is a chalcogenide.

23 (Currently Amended). A method comprising:

forming a breakdown layer between a pair of electrodes and increasing the likelihood that a breakdown will occur in one region rather than another region of said layer by damaging said one region and not damaging said other region.

24 (Original). The method of claim 23 including forming a phase change material between said electrodes.

25 (Original). The method of claim 23 including ion implanting said breakdown layer.

26 (Currently Amended). A memory comprising:

a breakdown layer between a pair of electrodes, said breakdown layer having a central region and a peripheral region between said electrodes, one of said central and said

peripheral regions being damaged such that a breakdown is more likely to occur in one of said regions than the other of said regions.

27 (Original). The memory of claim 26 including a phase change material between said electrodes.

28 (Original). The memory of claim 27 wherein said breakdown layer is ion implanted.

29 (Original). The method of claim 28 including a dielectric over a substrate, said dielectric having an aperture and said breakdown layer being formed in said aperture.

30 (Original). The memory of claim 29 including an electrode at the bottom of said aperture and another electrode over said aperture, said phase change material being between said electrodes.